Unit1

- KCL: current in = current out
- KCL: sum of voltage around loop = 0
  - negative => opposite direction
- Ohm's law: V = IR
- Resistance
  - series: R_eff = R1+R2
  - parallel: R_eff = (1/R1+1/R2)^-1
- Voltage divider: must be in series, V1 = V_tot * (R1/(R1+R2))

Unit2

- Gates
  - AND
  - OR
  - NOT
  - NAND
  - NOR
  - XOR
  - XNOR
- Design Goals
  - Minimize circuit size
    - reduce gates/inputs
  - Maximize speed/Minimize delay
    - path length
    - gate type
  - Minimize power
- Boolean Algebra
- Combinational Logic
  - outputs = f(current inputs)
  - memoryless
- Sequential Logic
  - outputs = f(current + past inputs)
  - stateful

Unit3

- base r to base 10
- base 10 to binary
- binary <=> oct <=> hex
- unique combinations
  - n bits in base r => r^n combinations
- approximations of powers of 2
  - 2^10 thousand Kilo
  - 2^20 million Mega
  - 2^30 billion Giga
  - 2^40 trillion Tera

Unit4

- bit fiddling
  - clear to 0 - AND
  - set to 1 - OR
  - invert - XOR

    - check - AND
- registers
    - DDRx
    - PORTx
    - PINx

Unit5

- use state to perform operations at different rates/intervals
    - A set of possible input values: {0, 1}
    - A set of possible states: {S0, S1, S2}
    - A set of possible outputs: {False, True}
    - An initial state = S0
    - A transition function:
        - {States x Inputs} -> the Next state
    - An output function:
        - {States x Inputs} -> Output value(s)